Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please amend claims 2-4 as follows:

1. (original): A method for power control in a scalable pipelined array processor comprising the steps of:

controlling the execution of instructions in processing elements (PEs) and in a sequence processor (SP) by examining an S/P bit of each instruction;

masking off one or more PEs;

where a PE is masked off, allowing only PE communication DSU instructions to be decoded by the masked off PE, the masked off PE providing cluster switch control information in response to decoding a PE communication DSU instruction; and

maintaining all other execution units in masked off PEs in an inactive state to conserve power.

2. (currently amended): The method of claim 1 further comprising ~~the steps of~~:

keeping the PEs off when an SP-only instruction is executing; and

gating ~~the~~ an array clock off to the PEs.

3. (currently amended): A method for power control in a scalable pipelined array processor comprising ~~the steps of~~:

configuring the scalable pipelined array as a 2 x 2 or smaller array processor, the scalable pipelined array processor having a plurality of processing elements (PEs), the plurality of PEs being connected to a cluster switch;

controlling the execution of instructions in the plurality of ~~processing elements (~~PEs~~)~~ and in a sequence processor (SP) by examining an S/P bit of each instruction;

masking off one or more of the plurality of PEs, with the masked off one or more of the plurality of PEs not executing any instructions, while the non-masked off PEs continue to communicate through the cluster switch without being effected by the masked off PEs; and

maintaining all execution units in masked off PEs in an inactive state to conserve power.

4. (currently amended): The method of claim 3 further comprising ~~the steps of~~:

keeping the PEs off when an SP-only instruction is executing; and

gating ~~the~~ an array clock off to the PEs.

Please add the following new claims.

5. (new): A method for power control in a scalable pipelined array processor comprising:

controlling the execution of instructions in the plurality of PEs and in a sequence processor (SP);

masking off one or more PEs;

where a PE is masked off, allowing only PE communication DSU instructions to be decoded by the masked off PE, the masked off PE providing cluster switch control information in response to decoding a PE communication DSU instruction; and

maintaining all other execution units in masked off PEs in an inactive state to conserve power.

6. (new): The method of claim 5 wherein the controlling step includes generating a HOLD_PIPE signal.